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Japanese Laid-Open Patent

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Application Number: SHO 57-38769

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Applicant: SEMICONDUCTOR ENERGY LABORATORY CO., LTD.

SPECIFICATION

1. Title of the Invention

Semiconductor Device

2. Scope of Claims

1. A semiconductor device in which a first electrode comprising a substrate or a conductive layer on said substrate, one conductive type of a first non-single crystal semiconductor layer formed on said electrode, a second and a third non-single crystal semiconductor layer having a lower impurity density than said semiconductor layer and a fourth semiconductor layer having a conductivity type opposite to the counterpart of the first semiconductor layer are laminated and formed, a semiconductor device characterized by comprising said second semiconductor layer and said third semiconductor layer, said second and third semiconductor layers being provided with a IP-junction, a IN-junction and a P-N-junction.

2. A semiconductor device according to claim 1 wherein said photo-electric converter is provided with either a PIN-N-junction and a NIP-P-junction from the light irradiation surface side.

3. A semiconductor device according to claim 1 wherein either a P-type

semiconductor or an N$^-$-type semiconductor has a P-type conductivity or an N-type impurity density of 7×10^{16} to 1×10^{18}cm^{-3} while an I-type semiconductor has an impurity density of 5×10^{16}cm^{-3}.

4. A semiconductor device according to claim 1 wherein said I-type semiconductor layer has a thickness of 100 to 2000 Å while said P$^-$-type or said N$^-$-type semiconductor layer has a thickness of 0.6 to 0.1 Å.

3. Detailed Description of the Invention

The present invention relates to a semiconductor device using a non-single crystal semiconductor, and more particularly to a semiconductor device having an IP$^-$-junction, an IN$^-$-junction and a PN$^-$-junction by laminating so-called substantially intrinsic semiconductor layer (hereinafter simply referred to as an I-layer or an intrinsic semiconductor layer) intrinsically or artificially free from laminate doping of a P-type or an N-type impurity and a P$^-$-type or an N$^-$-type semiconductor layer, the semiconductor device having a semiconductor layer for generating photo-electromotive force (hereinafter simply referred to as an active semiconductor layer) for generating electron-hole pair by light irradiation.

An object of the present invention is to provide an photo-electric converter providing a PINN-junction and NIPP-junction from the side of light irradiation surface to substantially lengthen a life time of a few carriers in an active semiconductor layer and to finally output a large amount of current.

The present invention relates to a method for fabricating a semiconductor device characterized by:

connecting and providing four reaction chambers for laminating a first, a second, a third and a fourth non-crystal semiconductor layers to form a PINN-

junction and a NIPP-junction in place of fabricating these semiconductor layers in the same reaction chamber;

forming a first semiconductor layer;

subsequently forming a second semiconductor layer on said first semiconductor layer without exposing to the atmosphere the substrate having a formed surface on an adjacent reaction chamber by repeating the aforementioned step;

forming a third semiconductor layer on the second semiconductor layer by repeating the aforementioned step; and

forming a fourth semiconductor layer on the third semiconductor layer by repeating the aforementioned step.

The present invention relates to a method for forming a semiconductor device by connecting the four reaction chambers. The present invention is intended to remove adhesives such as moisture, air or the like on the first semiconductor layer prior to the formation of the first semiconductor layer, and to provide a first preparatory chamber for shielding the atmosphere to prevent the contamination of the atmosphere (air, particularly oxygen and water) and a second preparatory chamber for preparatory heating, the second preparatory chamber being intended to remove adhesives on the substrate.

Heretofore, with the photo-electric converter having a PIN-junction formed by the laminating process using the plasma CVD, in particular, the glow discharge process, there are known patent applications entitled "Semiconductor Device for Generating Photo-electromotive Force" (Japanese Unexamined Patent Application No. HEI 51-890 and Japanese Unexamined Patent Application No. SHO 49-71739 filed on June 20, 1974) filed by the applicant of the present invention. Further, a patent application entitled "Semiconductor Device" (Japanese Unexamined Patent

Application No. SHO 52-16990) is also known. However, the aforementioned patent applications do not disclose at all the detailed items of an I-layer as an intrinsic semiconductor layer in these semiconductor device while indicating that the I-layer is a low impurity density layer compared with a P-type or an N-type semiconductor layer sandwiching the I-layer.

The present invention is concerned with an photo-electric converter fabricated by laminating semiconductor layers on the formed surface, characterized in that the inside of the photo-electric converter is formed by laminating at respective reaction chamber an I-type semiconductor layer having an impurity density of only $5 \times 10^{16}cm^{-3}$ or less, and a P--type or an N--type semiconductor layer doped with an impurity having a density of 7×10^{16} to $1 \times 10^{18}cm^{-3}$ so that respective impurities do not contaminate as a result of further investigation of the active semiconductor layer. As a consequence, the present invention is characterized in that this active semiconductor layer is opposed to an electron or a hole in a laminating manner. At the same time, the present invention is characterized in that a few carriers out of carriers generated by the light irradiation is likely to be drifted to the electrode, and the life time of carriers is prolonged.

Further, the present invention is characterized in that the first and the second preparatory chambers are provided to remove oxygen doped in the semiconductor so that the density of the oxygen is set to 1/3 of the conventionally known density of 1 to $20 \times 10^{11}cm^{-3}$ or less, and more preferably 1/10 to 1/50 thereof with result that a silicon oxide insulating component is removed, and the life time of carriers as the semiconductor is prolonged.

Further, a method for laminating independently each of semiconductor layers is described in a patent application entitled "Semiconductor Device"

(Japanese Unexamined Patent Application No. SHO 53-152887 filed on December 10, 1958) and a divisional application thereof entitled "A Method for Fabricating a Semiconductor Device" (Japanese Unexamined Patent Application No. SHO 56-55607 filed on April 15, 1981) both of which are filed by the applicant of the present invention. Although these patent applications describe an independent connecting mode plasma CVD, they do not describe that the active semiconductor layer is further divided into a plurality of layers to form an IP⁻-junction and an IN⁻-junction, or further developed IP⁻P⁻ junction, or a PIN⁻N-junction. The present invention provides a further development thereof and is characterized in that the conversion efficiency as the photo-electric converter is further improved by 4 to 6% from the conventional 6 to 8%/cm^2 to be set to 10 to 14%/cm^2 (an intrinsic conversion efficiency of 5 cm^2 at the illumination light having an AMI of 100 mV/cm^2).

In an photo-electric converter of the present invention, either the P-type or the N-type semiconductor layer, particularly either the P-type or the N-type semiconductor layer on the incident light side is formed into a wide energy band compared with the active semiconductor layer thereby preventing an increase in the loss of absorbed illumination light at the semiconductor layer.

As a semiconductor device in which this energy band is continuously joined and a window structure is provided with respect to either the P-type or the N-type semiconductor layer, a patent application entitled "A Semiconductor Device" filed by the applicant of the present invention (US Patent No. 4,239,554 published on December 6, 1980 and US Patent No. 4,254,429 published on March 3, 1981) is known. The present invention is a further development of the application of the invention filed by the applicant of the present invention.

The present invention provides an unpaired bond neutralization effect by allowing such a semiconductor layer to contain hydrogen or a halogen element such as fluorine, chlorine or the like for recombination center neutralization at a density of 0.1 to 20 mole% and alkaline metal element such as lithium or the like at a density of 10^{15} to $10^{17}cm^{-3}$. At the same time, the present invention is made of a laminating structure in which a semi-amorphous (half non-crystal) semiconductor (hereinafter referred to as a SAS) having a crystallinity (short range order crystallinity) with a size of 5 to 2000 Å typically 5 to 100 Å and an amorphous (non-crystal) semiconductor (hereinafter referred to as an AS) having no such short range order crystallinity are laminated in layers.

In accordance with the present invention, the N-type semiconductor layer on the light illumination side in the photo-electric converter is formed as SAS to reduce the absorption of the incident light, and further an intrinsic semiconductor adjacent to the aforementioned semiconductor layer is formed as an SAS. Then, the life time of the carriers on the incident light side is prolonged, and an intrinsic semiconductor layer in which AS or SA is contaminated in a step-like or a continuous manner is laminated, and an inside electric field is spontaneously provided to further the improvement of the photo-electric conversion efficiency.

With respect to the SAS, Japanese Unexamined Patent Application No. SHO 55-026388 filed on March 3, 1980 (semi-amorphous semiconductor) filed by the applicant of the present invention is known. Further, as an invention in which this SAS is used to provide a PIN-junction photo-electric converter, Japanese Unexamined Patent Application No. SHO 56-008699 filed on January 22, 1981 (photo-electric converter) is known.

The present invention will be explained hereinafter in conjunction with the

drawings.

Fig. 1 shows an outline of a plasma CVD system required for the practice of the present invention.

In other words, a substrate (1) is in parallel with the flow of a reactive gas flowing from the upward direction to the downward direction in reaction furnaces (25) through (28) in which an insulating holder, for example, a quartz holder (board) (2) is held, and the substrate (1) is placed in a parallel direction with respect to the discharge of the electrode with respect to a high frequency energy (4). Regarding the reactive gas, a silicon gas ($SixH_{14}$ x $\geqq 1$) is supplied from (5), (9), (13) and (17), diboran (B_1H_4) which is a P-type impurity is supplied from (6), phosphine (PH_4) which is an N-type impurity is supplied from (18), hydrogen or helium (He) which is a carrier gas is supplied from (8), (11), (16) and (20). Further, a dopant having a wide energy band, for example, methane (CH_4) is supplied from (7) and (19). Diboran which is diluted with 10 to 100 PPM with silane is supplied from (10) and (14). Further, in the same manner, phosphine which is diluted to 10 to 100 PPM with silane is supplied from (11) and (15).

These gases are supplied from a discharge port to the reaction chamber of the reactive gases and electrodes (51), (52) and (53) for the plasma generation to reaction chambers (25), (26), (27) and (28). When these reactive gases are discharged to the reaction chambers, electro-magnetic energy is applied to activate and dissolve these gases with the result that reaction products are accumulated on the formed surface. In this reaction chamber, electro-magnetic energy such as direct current of up to 20 MHz, for example direct current having a frequency of 500 KHz, and 13.56 MHz is added to the electrodes (2) and (3). Further, the

substrate (1) having a formed surface is heated to 100 to 500℃, typically to 200 to 300℃ with an infrared ray furnace (4) so that a large number of substrates can be treated.

In the beginning, the substrate (1) is placed in a preparatory chamber (23), and the preparatory chamber (23) is evacuated with a rotary pump (30). To set the pressure in the preparatory chamber (23) to the atmospheric pressure, nitrogen is introduced from (21). After the preparatory chamber was evacuated, the substrate (1) is moved to the third preparatory chamber provided adjacent to the first preparatory chamber and heated to 200 to 400℃ with a infrared ray lamp by opening the gate (56). After the substrate (1) is moved to the third preparatory chamber, the gate (56) is closed again. After the pressure in the first preparatory chamber is set to the atmospheric pressure by introducing nitrogen from (21), another substrate is introduced. By the repetition of the aforementioned operations, the substrate in the first preparatory chamber is moved and introduced into the second preparatory chamber while the substrate in the substrate (1) in the second preparatory chamber (24) is moved and introduced into the first reaction chamber (23). Further, the removal of the absorbed oxygen and water by evacuation and heating after removal of the air by the evacuation in the first preparatory chamber enables to lower the density of oxygen in the semiconductor layer further to 1/3 of the conventionally known level of 1 to 3 x 10^{18} cm^{-3} or less, typically even to 1 x 10^{17} cm^{-3} to 5 x 10^{15} which is 1/10 or 1/30 of the conventional level.

Needless to say, an attempt is made to secure the vacuum leak from the outside in each reaction chamber to

10^{-3} torr or less.

As described above, a $SixO_{1-x}$ film ($0 < x < 1$) having a P-type is formed to a thickness of 200 Å or less, typically 30 to 160 Å followed by evacuating the first and the second reaction chamber to move the substrate having a formed surface to the second reaction chamber. The substrate placed in the second reaction chamber (26) is moved to the third reaction chamber (27), the substrate placed in the third reaction chamber (27) is moved to the fourth reaction chamber (28), the substrate placed in the fourth reaction chamber (28) is moved to the third preparatory chamber (29), and the substrate placed in the third preparatory chamber is taken out from another gate (57) to the outside after the gate (56) is completely closed.

Fig. 2(A) shows a vertical cross sectional view of the second reaction chamber (26). After the P-type first semiconductor layer (44) is formed, an I-type second semiconductor layer (45) is formed to a thickness of 100 to 2000 Å, typically to a thickness of 200 to 500 Å When this I-type layer forms the second semiconductor layer, an impurity for forming the first semiconductor layer contaminates into the I-layer to a depth of 50 to 100 Å the second semiconductor layer is formed to a thickness of 100 Åor thicker. An effort has been made so that the P-type impurity and the N-type impurity does not directly contaminate with each other at a density of 5×10^{16} cm^{-3} or more.

This I-type semiconductor layer is extremely important for forming a depletion layer and for promoting the movement of carriers to the electrode by a drift.

Further, after the above-mentioned operation, in the third reaction chamber (27), the N-type third semiconductor layer (46) shown in Fig. 2(A) is formed to a thickness of 0.1 to 0.6 ŧ. Further, in the fourth reaction chamber (28), the N-type fourth semiconductor layer (47) is formed to a thickness of 100 to 500 Å This

semiconductor layer is also formed into a $SixO_{1-x}$ ($0 < x \leqq 1$) in which this Eg is set to 1.8 to 2.5 eV to provide the BSF (depletion layer electric field in the reverse direction) to a few carriers. Further, in the I-layer (45) and the N-layer (46), the aforementioned amorphous silicon is used to set to 1.5 to 1.8 eV.

After four semiconductor layers are formed as described above, an organic resin mold (49) such as epoxy, polyamide or the like coats the semiconductor layers to a thickness of 100 to 500 Å for the electrode (48) and for the improvement of the moisture resistance.

Referring to Fig. 2(A), as the substrate, a light transmitting substrate (40), for example, a glass or polyamide resin is used. Al or Cu is provided on a typical substrate or a bulk thereof doped with Ni having a depth of 5 to 20 μ, or No added with B or P to provide an embedded electrode (41). Further, on the upper surface, a transparent conductive film (43) may be a two-layer film formed by laminating ITO (indium oxide + 3 to 10% of tin oxide) with tin oxide, antimmon oxide or a mixture thereof.

This transparent conductive film is formed to a thickness of 50 to 200 Å in such a manner that when the semiconductor contacting the transparent conductive film is a P-type semiconductor as seen in this embodiment, the transparent conductive film contacts an antimmon oxide (Sb_2O_2 or Sb_4O_2) which is a V value transparent conductive film, and the ITO is provided on the base of this conductive film so as to improve the conductivity of this conductive film, which contribute to the improvement of the conversion efficiency of the photo-electric converter, and particularly to an increase in current. Then, when the ITO is allowed to contact the P-type semiconductor, the current which was on the order of 5 to 10 mA can be largely increased to 13 to 20 mA/cm^2. As a consequence, antimmon becomes a

recombination center of a hole in the P-type semiconductor with the result that a electric series resistance at this interface can be lowered.

The energy band width corresponding to Fig. 2(A) obtained in the aforementioned manner is provided by adding corresponding reference numerals in Fig. 2(B).

As apparent from the drawings, the active semiconductor layers (41) through (46) can efficiently supply holes which are a few carriers in this case to the P-type semiconductor layer (44) with a high potential difference between (44) and (46). In particular, to provide a spread of the depletion layer at an intrinsic semiconductor layer (48) located in the vicinity of the illumination light and a high electric field strength, an N-type semiconductor layer (46) is provided so that the carrier generated by the light irradiation at the semiconductor layer (46) provides a drift of few carriers to the P-type semiconductor layer including an aid of BSF effect. As a consequence, although only an efficiency of 5 to 7% /cm^2 can be obtained in the conventionally known PIN semiconductor, 10 to 12% higher conversion efficiency can be obtained with an AMI by adopting a PIN-N-junction structure. Further, with a large substrate having an area of 10 cm^2, 7 to 10% practical conversion efficiency can be obtained at an open voltage of 0.9 to 0.95 V and a short circuit current of 16 to 20 mA including the aid of the auxiliary electrode (41).

Fig. 3 shows an example in which the substrate (40) is made conductive and is formed of, for example, stainless steel. In the same manner as Fig. 2(A), on the upper surface of the substrate, the first semiconductor layer, the second semiconductor layer, the third semiconductor layer and the fourth semiconductor layer are provided in such a manner that the semiconductor layers and the P-type

semiconductor layers (44), (45), (46) and (47) are laminated on each other. The semiconductor layers are provided with the ITO transparent conductive film (45), an auxiliary electrode (41) and the resin mold (49).

The corresponding energy band view taken along line A-A' is shown in Fig. 3(B). It is different from the case shown in Fig. 2(A). Due to light irradiation from the upward direction, the N-type semiconductor layer (47), the I-type semiconductor layer (46) and the P⁻-type semiconductor layer (44) are provided. In such a case, at the time of the formation of the film, the P-type semiconductor layer has an extremely low impurity density of 5×10^{16} to $1 \times 10^{19} cm^{-3}$ so that it is impossible to form 5 to 10 PPM (hydrogen dilution) due to the reaction between diboran and bomb in the bomb. Consequently, the present invention is further characterized by using bomb in which 10 to 100 PPM of diboran is doped in silane. In this manner, the P⁻-type semiconductor layer (45) with controllability can be prepared. Here, the contamination of the P-type impurity by automatic doping from the first semiconductor layer is inhibited. Consequently, in accordance with the present invention, as shown in Fig. 1, the first reaction chamber (25) for the P-type semiconductor layer and the second reaction chamber for the P⁻-type semiconductor layer are made independent. In particular, when carbon is doped into the P-type semiconductor layer (44), it is extremely important that the carbon partially (locally) contaminates the P⁻-type second semiconductor layer, thereby preventing the electric conductivity. Consequently, the second semiconductor layer (45) comprises a primary component such as germanium or a mixture thereof. Then an attempt is made to prevent as much as possible the contamination of either carbon, oxygen or nitrogen into the semiconductor layer at a density of $3 \times 10^{19} cm^{-3}$ or more which worsens the electric recombination

degree.

Thus, in the case as shown in Fig. 3(B), the conversion efficiency of more than 10% can be obtained in the same manner as shown in Fig. 2.

Other methods for fabricating the semiconductor are the same as described with respect to Figs. 1 and 2.

In the above description, the semiconductor layer incorporates one PIN·N junction or one NIP·P junction. However, the above process is further repeated to continuously connect to a PIN·NPIN·N junction or a PIN·NPIN junction from the side of the light irradiation surface so that the front IN· active layer is set to 1.6 to 1.8 eV with the amorphous Bi while the rear side is set to 1.0 to 1.6 eV with $SixO_{1-x}$ ($0 \leqq X \leqq 1$) to attempt to increase an open voltage. Further, the same thing holds true of the case in which the NIP·P junction, the NIP·PNIP·P junction, or the NIP·PNIP junction is adopted with respect to NIP·P·junction.

As apparent from the above explanation, in accordance with the present invention, the semiconductor layer is formed of IN junction, IP junction, the N·P·· P· junction, the P·N··N· junction, the IP·P·· junction, or the NIP·PNIP junction so that the semiconductor layer has a lower impurity density than a P-type or an N-type semiconductor layer in the prior art. Additionally, when the semiconductor layer is formed of IN junction, the density of oxygen, carbon and nitorogen is set to 3 x 10^{17}cm or less of a measurment by IMA. Further, the contamination of II value impurity and V value impurity are avoided. Additionally, the life time of a few carriers is prolonged by providing either P^+ or N· type. Further, all of I·type, P^+·type and N··type are independently formed in the reaction chamber with the result that a large area type photo·electric converter can be fabricated having a high conversion efficiency of more than 10%. In this respect, it is believed that the

industrial value of the photo-electric converter of the present invention is not small.

4. Brief Description of the Drawings

Fig. 1 shows an outline of a fabrication of a semiconductor device used in the present invention.

Figs. 2(A) and 3 (A) show vertical cross sectional views of the photo-electric converter of the present invention.

Figs. 2(B) and 3(B) show energy band views corresponding to Figs. 2(A) and 3(A).

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⑭半導体装置

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明　細　書

1. 発明の名称

半導体装置

2. 特許請求の範囲

1. 基板または基板上の導電層よりなる第1の電極と、該電極上に一導電型の第1の非単結晶半導体層と、該半導体層に比べて低不純物濃度の第2、第3の非単結晶半導体層と、前記第1の半導体層とは逆導電型の第4の非単結晶半導体層とを積層して設けた光電変換装置において、前記第2および第3の半導体層がI型、I型、P型接合を有して設けられたことを特徴とする半導体装置。

2. 特許請求の範囲第1項において、光電変換装置は光照射面側よりPIN型またはNIP接合を有して設けられたことを特徴とする半導体装置。

3. 特許請求の範囲第1項において、P型またはN型半導体はPまたはN型の導電型用の不純物濃度が 7×10^{17}～1×10^{20} cm^{-3} を有し、I型半導体は 5×10^{17} cm^{-3} 以下の不純物濃度を有することを特徴とする半導体装置。

4. 特許請求の範囲第1項において、I型半導体層は100～2000Åの厚さを有し、P型またはN型の半導体層は0.6～0.1μの厚さを有することを特徴とする半導体装置。

3. 発明の詳細な説明

本発明は非単結晶半導体を用いた半導体装置特に光照射により電子・ホール対を発生する光起電力発生用半導体層（以下単に活性半導体層という）を有する真性または人為的にP型またはN型の不純物を故意的に添加しないいわゆる実質的に真性の半導体層（以下単にI層または単に真性半導体層という）およびP型またはN型半導体層を積層してPI, IN, PN接合を有せしめた半導体装置に関する。

本発明は光電変換装置の光照射面側よりPIMM MIPP接合を有せしめ、活性半導体層における少数キャリアのライフタイムを実質的に長くして、ひいては大電流出力を有せしめることを目的としている。

本発明は第1、第2、第3、第4の非単結晶半導体層を積層して、PIMM, MIPP接合を有せしめるにあたり、これらの半導体層を同一反応室を用いて作製するのではなく、それぞれ独立した4個の反応室を連結して具備せしめ、第1の半導体層を形成した後、隣の反応室に被形成面を有する基板を大気にふれさせることなく第1の半導体層上に第2の半導体層を積層して形成せしめ、かかる工程を順次くりかえすことにより第1の半導体層上に第2の半導体層を、また第2の半導体層上に第3の半導体層を、第3の半導体層上に第4の半導体層を形成せしめる半導体装置の作製方法に関する。

本発明は4つの反応室を連結して有する半導体装置作製方法に関し、その第1の半導体層を形成するに先立ち、その半導体層上に水分、空気等の吸着物を除去し、さらに反応室に大気（空気特に酸素、水）の混入がないように、大気との遮断用の第1の予備室と、基板上の吸着物除去用の予備加熱用の第2の予備室を設けることを目的としている。

従来プラズマCVD法特にグロー放電法を利用し、PIN接合を積層法にて有する光電変換装置に関しては、本発明人の出願になる「光起電力発生用半導体装置」（昭49.6.20出願　特開昭51—890　特願昭49—71739）が知られている。また　半導体装置（特開昭52—16990）も知られている。しかしこれらの半導体装置における活性半導体層としてのI層は、このI層をはさむPまたはN型半導体層に比べて低不純物濃度層であることを指摘しながらも、さらにその細目については全く開示していない。

本発明は半導体層を被形成面上に積層して作製する光電変換装置において、この活性半導体層をさらに検討した結果、その内部を$5\times10^{16}cm^{-3}$以下の不純物濃度しかないI型半導体層と、$7\times10^{16}\sim1\times10^{18}cm^{-3}$の濃度の不純物が添加されているPまたはN型半導体層をそれぞれ独立した反応室で積層して形成し、お互いの不純物が混入しあわなくせしめたことを特徴としている。この結果、この活性半導体層を電子またはホールと積層的に対立させ、かつ光照射により発生したキャリアのうちの少数キャリアを電極へドリフトさせやすく、ひいてはそのライフタイムを長くせしめたことを特徴とする。

さらに本発明はこの半導体中に添加された酸素の濃度を第1および第2の予備室を設け、そこで除去することにより、従来知られていた$1\sim20\times10^{18}cm^{-3}$の濃度よりさらに1/3以下好ましくは1/10~1/50としたことにより、半導体をその中に酸化珪素絶縁性成分を除去し、より半導体としキャリアのライフタイムを長くしたことを特徴としている。

また半導体層をそれぞれ独立に積層する方法は本発明人により　半導体装置（特願昭53—152887　昭53.12.10出願）およびその分割出願　半導体装置作製方法（特願昭56—55607　昭56.4.15）に記されている。しかしこれらは独立連結方式のプラズマ気相法が記されていても、やはり活性半導体層をさらに複数層にわけ、そこをIP, IN接合、さらにそれを発展させたPIPP, PINNを形成することについての記載はない。本発明はこれをさらに発展せしめ、光電変換装置としての変換効率を10~14%/cm²(AM1 100mW/cm²の照射光における$5cm^2$の真性変換効率）を有せしめ、従来の6~8%/cm²よりもさらに4~6%も向上せしめたことを特徴としている。

本発明における光電変換装置において、Pまたは N型半導　層特に入射光側のPまたはN型半導体層を活性半導体層に比べて広いエネルギバンド巾とし、その半導体層での照射光の吸収

損失の増加を防いでい[redacted]

このエネルギバンド構造を連続接合し、PまたはN型の半導体層に対し窓構造を設けたものとして、本発明人の出願になる　半導体装置（米国特許　4,239,554　1980.12.6発行　米国特許　4,254,429　1981.3.3発行）が知られている。本発明はかかる本発明人の発明になる出願をさらに発展させたものである。

本発明はかかる半導体層に再結合中心中和用の水素、フッ素または塩素の如きハロゲン元素を0.1～20モル%の濃度に、またリチューム等の如きアルカリ金属元素を10^{17}～$10^{20}cm^{-3}$の濃度に含有せしめて、不対結合手中和効果を有せしめるもに、5～2000A代表的には5～100Aの大きさの結晶性（ショートレンジオーダの結晶性）を有するセミアモルフアス（半非晶質）半導体（以下SASという）とかかるショートレンジオーダの結晶性を有さないアモルフアス（非晶質）半導体（以下ASという）とが層状に積層構造を有して設け[redacted]たものである。

本発明は特に光電変換装置における光照射面側のN型の半導体層がその領域での入射光の吸収性を少なくするためSASとし、さらにそれに隣接した真性半導体層をSASとし、入射光側でのキャリアのライフタイムを長くし、さらにこのSAS上面に真性の階段状または連続的にASまたはASを混入させた半導体層を積層して内部電界を自発的に設け、光一電気変換効率の向上を促したものである。

SASに関しては、本発明人の出願になる特願昭55—026388，855.3.3出願（セミアモルフアス半導体）が知られている。さらにこのSASを利用してPIN接合型の光電変換装置を設けた発明として、本発明人の出願になる特願昭56—008699，856.1.22（光電変換装置）が知られている。

以下図面に従つて説明する。

第1図は本発明を実施するのに必要なプラズマCVD装置の概要を示す。

すなわち基板(1)は絶縁性ホルダ例えば石英ホルダ（ボート）(2)が保持された反応炉(4)～(4)中に上方向から下方向への反応性ガスの流れに平行であり、かつ高周波エネルギ(6)に対する電極(2)(3)の放電に対し平行方向に設置させている。反応性気体は珪化物気体（Si_nH_{2n+2}　$n \geq 1$）を(5),(9),(13),(17)より、またP型不純物であるジボラン（B_2H_6）を(6)より、N型不純物であるフオスヒン（PH_3）を(18)より、キヤリアガスである水素またはヘリューム（He）を(8),(12),(16),(20)より供給した。また広いエネルギバンド巾とするための添加材例えばメタン（CH_4）を(7),(11)より供給する。シランにより10～100PPMに希釈されたジボランを(10),(14)よりまた同様に10～100PPMのフオスヒンを(15),(19)より供給する。

これらを反応性気体の反応室への噴出し口であつて、かつプラズマ発生用の電極(51),(52),(53),(54)より反応室(4),(4),(4),(4)に供給している。この反応性気体が反応室に放出されると、電磁エネルギが加えられ、それらの気体を活性化、分解して反応生成物が被形成面上に蒸積される。この反応室では直流～20MHz例えば直流、500KHz、13.56MHzの周波数の電磁エネルギを電極(2)(3)より加えた。さらに被形成面を有する基板(1)に赤外線加熱炉(6)により100～600°C代表的には200～300°Cに加熱し、多量の基板処理ができるようになつた。

基板(1)は最初第1の予備室(4)に挿入され、ロータリーポンプ(30)にて真空引きされた。この予備室を大気圧にするには(31)より窒素を導入した。この予備室が真空引きされた後、その隣りに設けられた200～400°Cに赤外線ランプにて加熱された第3の予備室にゲイト(35)を開けて移し、移した後再びゲイト(35)を閉め、第1の予備室は(31)より窒素を導入し大気圧とした後、別の基板が導入される。かくの如きくりかえしにより、第1の予備室の基板は第2の予備室に、第2の予備

室(24)の基板は第1の反応室(41)に漸次移相して導入される。さらにこの第1の予備室で真空引をして大気を除去した後、第2の予備室で吸着酸素、水を真空加熱により除去することは、半導体層中の酸素の濃度を従来より知られた1～3×10^{18}cm^{-3}よりもさらに1/3以下代表的には1/10～1/30の1×10^{17}～5×10^{17}cm^{-3}にまで下げることができた。

もちろん各反応室においても、外部よりの真空リークは10^{-7}torr以下を保障できるように務めている。

以上の如くにして第1の反応室において、被形成面上に1.6～2.8eVのエネルギバンド巾を有するP型の導電型を有するSi$_x$O$_{1-x}$(0<x<1)を200A以下代表的には30～150Aの厚さに形成した後、第1および第2の反応室を真空引をして、この被形成面を有する基板を第2の反応室(42)に移相した。この時第2の反応室に設置された基板は第3の反応室(43)に、第3の反応室(43)の基板は第4の反応室(44)に、第4の反応室の基板は第3の予備室(53)に移相し、第3の予備室の基板はゲイト(56)を完全閉にした後、他のゲイト(57)より外部に出される。

第2の反応室(42)においては、第2図(A)にその縦断面図が示されているが、P型の第1の半導体層(44)が形成した上にI型の第2の半導体層(45)が100～2000Aの厚さ代表的には200～500Aの厚さに形成される。このI層は第2の半導体層を形成する際、第1の半導体層を生成する不純物が50～100A混入するため、100A以上形成させ、P型用の不純物とN型用の不純物とが5×10^{17}cm^{-3}以上の濃度で直接に混合しないように務めた。

このI型半導体層は空乏層を形成させ、ここでのキャリアの電極へのドリフトによる移動を助長させるためにきわめて重要である。

さらにこの後第3の反応室(43)にて、第2図(A)におけるN型の第3の半導体層(46)を0.1～0.6μの厚さに形成させた。さらに第4の反応室(44)にてN型の第4の半導体層(47)を100～500Aの厚さに形成させた。この半導体層をもBSF(逆方向の空乏層電界)を少数キャリアに与えるため、このEgを1.8～2.5eVとしたSi$_x$O$_{1-x}$(0<x≦1)とした。またI層(45)、N$^+$層(46)は前記した非単結晶シリコンを用い1.5～1.8eVとした。

以上の如き4つの半導体層を積層した後、電極(48)および耐湿性向上のため、エポキシ、ポリイミド等の有機樹脂モールド(49)を100～500μの厚さにオーバーコートをした。

第2図(A)において、基板は透光性基板(40)例えばガラス、ポリイミド樹脂を用い、そこに3～20μの厚さのNi、Ni中にB、Pが添加された代表的またはそのバルクにAl、Cuが設けられ、うめこみ補助電極(41)を設けた。さらにこの上面に透明導電膜(43)を設けている。この透明導電膜はITO(酸化インジューム+3～10%酸化スズ)と酸化スズ、酸化アンチモンまたはその混合物を積層して2層膜としていい。

この透明導電膜はこれに接する半導体がこの実施例の如くP型半導体にあつてはV価の透明導電膜である酸化アンチモン(Sb$_2$O$_3$またはSb$_2$O$_5$)を50～200Aの厚さにそれに接する如くにして形成し、ITOはこの導電膜の導電性を向上させる如くにその下地に設けることが光電変換装置の変換効率の向上特に電流の増大に大きく寄与していた。そしてITOをP型半導体に接せしめる時、5～10mA/cm^{2}の電流までであつたものが13～20mA/cm^{2}ときわめて大きくできた。これはアンチモンがP型半導体のホールの再結合中心となり、この界面での電気的な直列抵抗を下げることができた。

以上の如くにして得られた第2図(A)に対応したエネルギバンド巾を第2図(B)にその番号を対応して設けている。

この図面より明らかな如く、活性半導体層

(41)～(46)はこの場合の少[redacted]ヤリアであるホールをP型半導体層(44)に(44),(46)間の高い電位差により効率よく供給せしめている。特に照射光近くにある真性半導体層(45)での空乏層のひろがりおよび高い電界強度を有せしめるためN型半導体層(46)を設け、さらにこの(46)で光照射により発生したキャリアはBSF効果の助けを含めて少数キャリアをP型半導体層にドリフトさせたものである。その結果、従来より知られた単なるPIN半導体においては5～7%/cm²までの効率しか得られなかつたものが、PINN型構造とすることにより、10～12%の高い変換効率をAM1にて得ることができた。さらに100cm²の大面積基板においても、(41)の補助電極の助けを含めて開放電圧0.9～0.95V、短絡電流16～20mA/cm²、7～10%の実用変換効率を得ることができた。

第3図は基板(40)を導電性とし、例えばステンレスとしたものである。この上面に第2図(A)と同様に第1、第2、第3、第4の半導体層を(44),(45),(46),(47)[redacted]層して設け、ITOの透明導電膜(45)補助電極(51)樹脂モールド(49)により設けている。

A—A'における対応エネルギバンド図を第3図(B)に示している。この場合は第2図(A)と異なり、上方向よりの光照射のためN(47)I(46)P⁻(45)P(44)としている。この場合P⁻はその被膜形成の際その不純物濃度が5×10¹⁶～1×10¹⁷cm⁻³ときわめて低いため、ボンベ中で5～10PPM（水素希釈）を作ることがジボランとボンベとの反応により不可能である。このため本発明においては、シラン中に10～100PPMのジボランを添加したボンベを用いていることが他の特徴である。かくして制御性を有するP⁻半導体層(45)を作ることができた。この中に第1の半導体(44)よりのオートドーピングによるP型不純物の混入を禁止するため、本発明においては第1図に示す如くP型半導体層(44)用の第1の反応室(21)とP⁻型半導体層用の第2の反応室(22)とを独立にしている。特にP型半導体層(44)に炭素を添加した場合、この炭素が部分的（局部的）にP⁻の第2の半導体層に混入し、電気的導電性を妨げることを防ぐことはきわめて重要である。このため(45)の第2の半導体層は珪素、ゲルマニューム[redacted]またはその混合体を主成分とし、炭素、酸素、窒素が3×10¹⁹cm⁻³以上の濃度に混入して電気的[redacted]濃度を悪くしないように務めた。

かくして第3図(B)の如き場合においても、第2図と同様の10%をこえる変換効率を得ることができた。

第3図の他の製造方法については第1図、第2図において述べたことと同様である。

以上の説明において半導体装置はPINまたはNIPP接合を1つ有せしめた。しかしこれをさらにくりかえし、光照射面側よりPINPINまたはPINPIN接合[redacted]し、前側のI活性層を非単結晶のSiにより1.6～1.8eVとし後側をSi$_{1-x}$Ge$_x$ (0≦x≦1)により1.0～1.6 eVとして開放電圧の増大に務めてもよい。またNIPPに関し、NIPPNIPP接合、NIPPNIP接合とした場合も同様である。

以上の説明より明らかな如く、本発明においては活性半導体層をI[redacted]、IFとし、従来より単にPまたはNの半導体層よりも低不純物濃度としたというのではなく、その中における電流防害要素である酸素、炭素、窒素を3×10¹⁹cm⁻³以下とし、さらに光照射面側でのI層中でのII価およびV価の不純物の混合をさけ、加えてP⁻またはN⁻とすることにより少数キャリアのライフタイムを長くさせたこと、さらにこのI、P⁻またはN⁻をそれぞれ独立に反応室で形成する等のすべてを一体化することにより、初めて10%をこえる高い変換効率を有す大面積型光電変換装置を作ることができる。この点でその工業的価値は少なくないものと信ずる

4.図面の簡単な説明

第1図は本発明に用いられた半導体装置製造

装置の概要を示す。

第２図、第３図において(A)は本発明の光電変換装置のたて断面図を示し、また(B)は(A)に対応したエネルギバンド図を示している。

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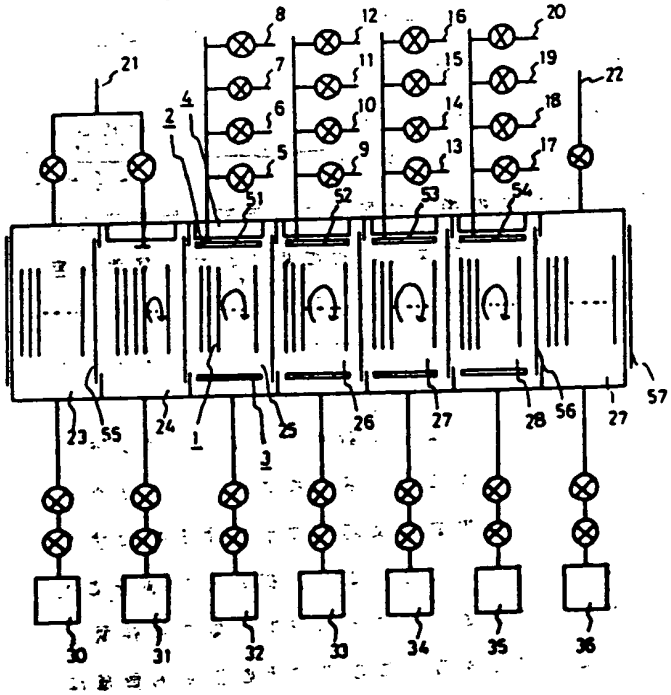
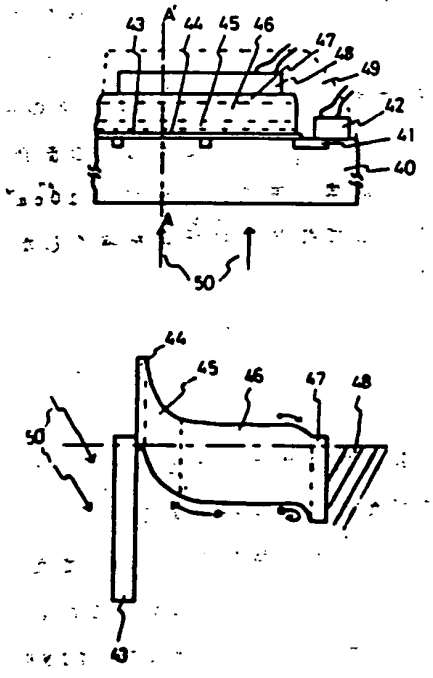
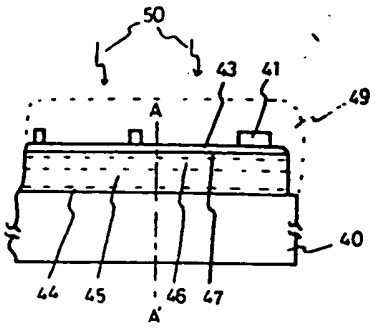


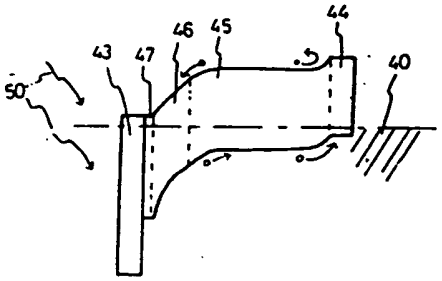
第１図



第２図



(A)



(B)

第3図